Analysis and Performance of BGA Interconnects for RF Packaging

D. Staiculescu[1], A. Pham[1], J. Laskar[1], S. Consolazio[2] and S. Moghe[2]

[1]Georgia Institute of Technology
Packaging Research Center
School of Electrical and Computer Engineering
791 Atlantic Drive
Atlanta, GA 30332-0250

[2]Northrop Grumman Corporation
600 Hicks Road
Rolling Meadows, IL 60008-1098

Abstract

We present the development of a lumped element model for the BGA transition using both measurements and simulations results. Measurements of the test structure are used to generate a circuit model for a single bump configuration. This model is used to calibrate EM simulations of the bump geometry. Furthermore, the effect of the bump diameter on the equivalent circuit model is presented. This model approach is scaleable and extendible to a more global behavior of BGA interconnects for RF packaging.

Introduction

Ball Grid Arrays (BGA) have received great attention as a low-cost, high density microwave integrated system interconnection solution [1]. The BGA multilayer structures have the advantages of reduced size and weight, possibility of mounting cheap ceramic substrates on PCB, compatibility with automatic manufacturing and minimized electrical path to the mother-board. Therefore, the modeling and characterization of BGA packages to microwave frequencies is of great practical interest.

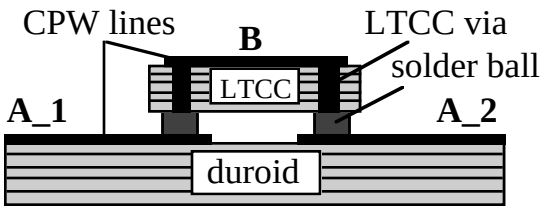
This paper presents the first comprehensive approach for characterization of microwave BGA's. A scaleable lumped-element circuit model up to 12 GHz and extendible to higher frequency is presented. The demonstration of the equivalent circuit shows the variation of the lumped element values with the horizontal diameter of the bump.

Approach

In order to obtain the equivalent circuit model for the BGA interconnect, a test structure has been designed to mount a Low Temperature Cofired Ceramic (LTCC) substrate on a Duroid printed circuit board (PCB). A schematic of the test structure is shown in fig. 1a. The PCB consists of two 50 ohm coplanar waveguides (CPW) (A_1 and A_2) on a low-cost Duroid multilayer substrate. A 50 ohm CPW transmission line (B) on LTCC multilayer substrate is soldered to the PCB using two balls. A top picture of the test structure is shown in fig. 1b.

The study of the loss and reflection due to the ball interconnect is done using the equivalent circuit model in fig. 2, which is similar to the configuration for a flip-chip transition [2]. C_1 denotes the discontinuity capacitance at the chip, C_2 the discontinuity capacitance at the mother-board, L_1 the inductance of the bump, and R_1, R_2, R_3 model the loss in the interconnection.

0-7803-4471-5/98/$10.00 (c) 1998 IEEE



ball height = 10 mil
ball width = 10 mil
duroid thickness = 5 x 10 mil
LTCC thickness = 5 x 3.6 mil

Fig. 1a. Schematic of the interconnection structure - side view

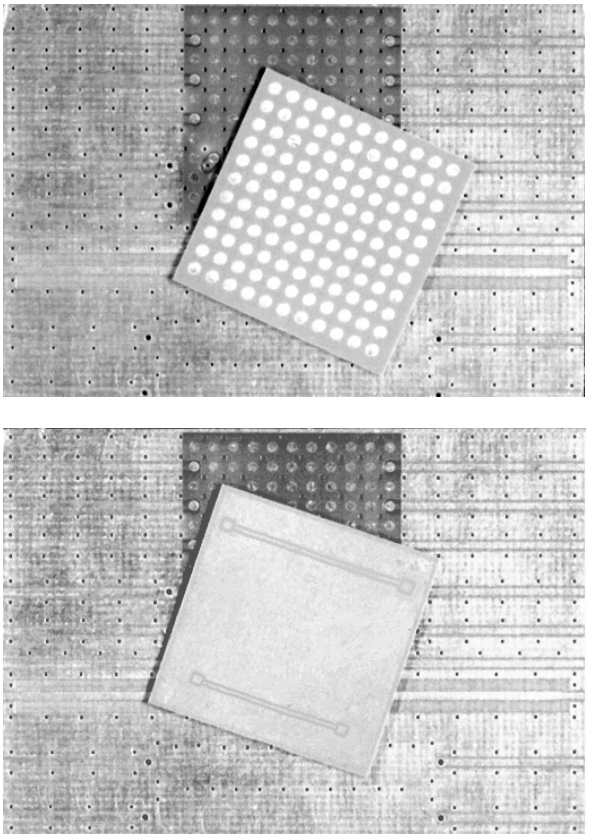


Fig. 1b. Test structure - top view.

The approach for deembeding the effect of the interconnection is presented in fig. 3. The values of the lumped elements are obtained by matching the measured S-parameters of the overall attached structure to the cascaded CPW transmission lines, LTCC vias and bump model, as presented in the block diagram in fig. 4.

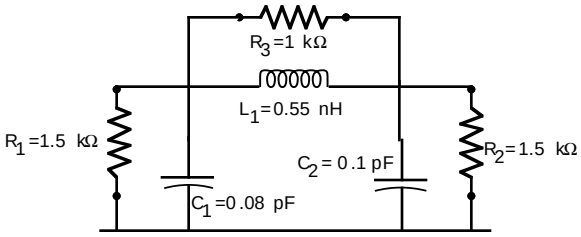


Fig. 2. Lumped element circuit model

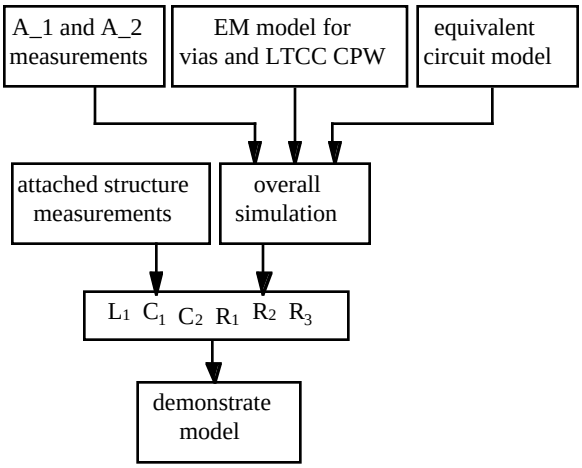


Figure 3. Deembeding technique

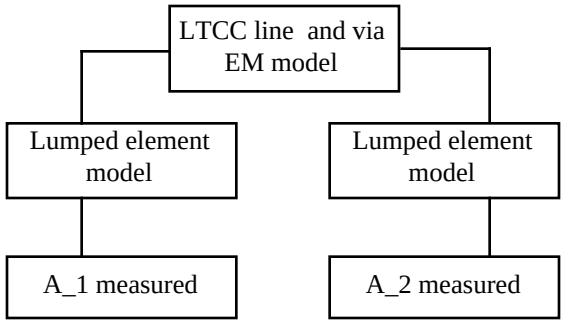


Fig. 4. Block diagram

The LTCC grounded CPW and the two LTCC vias have been simulated using SONNET EM simulator. The on-wafer measurements have been taken with an HP85109C network analyzer. The on-wafer line-reflect-match (LRM) calibration has been

performed on a Cascade Microtech impedance standard substrate.

Experimental results

The values of the circuit elements are determined by optimizing the circuit until the modeled and measured S-parameters are well correlated. Fig. 2 shows the lumped elements values as the result of the presented deembeding technique. Excellent correlation between measured and simulated S-parameters of the overall attached structure is shown in fig. 5.

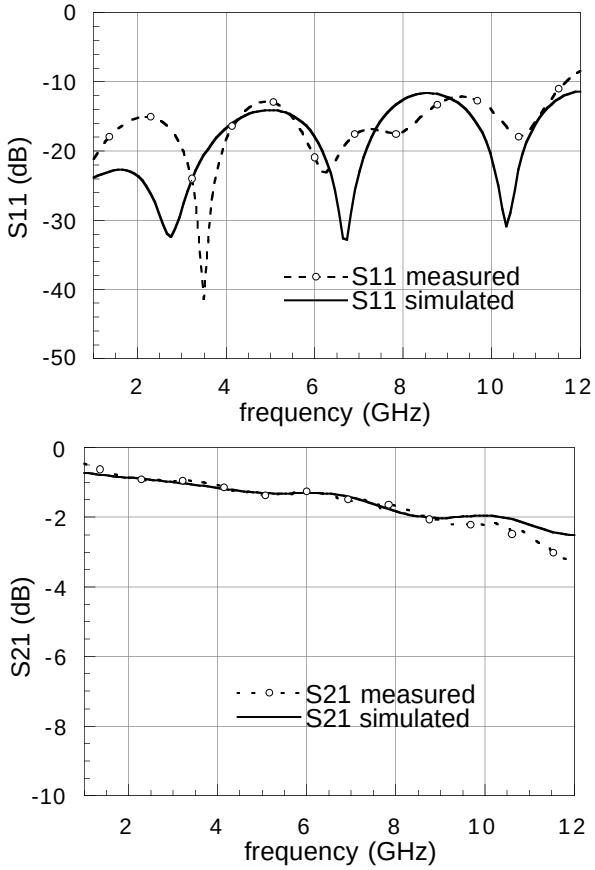


Fig. 5. Optimization result

For a single bump, the comparison of the equivalent circuit model to the simple via EM simulation is presented in fig. 6.

Application of this method is demonstrated by analyzing the effect of the via horizontal diameter on the elements of the equivalent circuit model. For several diameters of the bumps, the variation of the reactive elements in the model is presented in fig. 7.

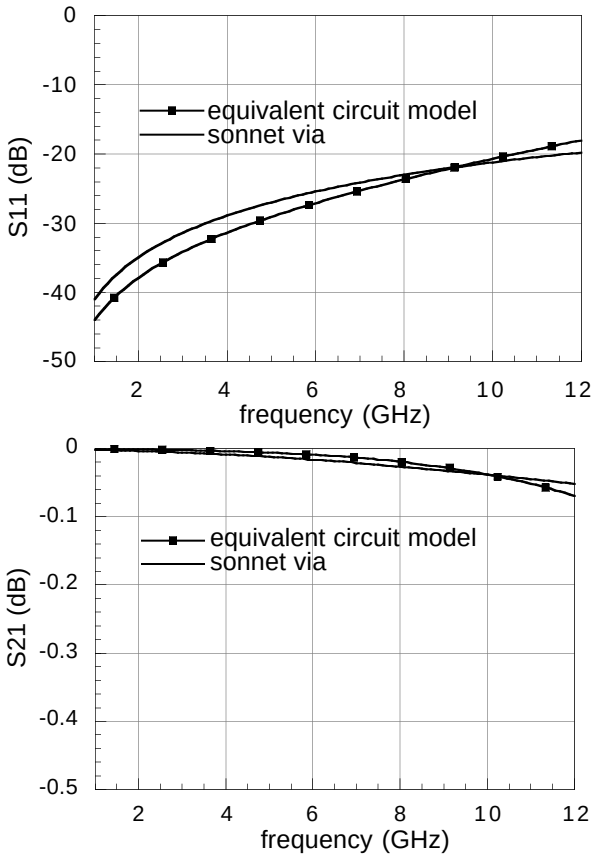


Fig. 6. Demonstration of the equivalent circuit.

Conclusion

The study and model of the high frequency behavior of the ball interconnects give the possibility to accurately and easily characterize BGA packages. The accurate microwave measurements of an attached structure are compared with simulation of the modeled circuit, which contains the measured and simulated cascaded S-parameters of the interconnected CPW's and the circuit models for bumps and vias. The applicability of the model is demonstrated by analyzing the effect of bump diameter on the lumped elements values.

The important issue determining the applicability of this approach is the coupling of the EM modeling/analysis with microwave measurements. This makes the method very flexible and extendible up to higher frequencies. Using this approach for various configurations can relate the ball model to physical attributes of the circuit, leading to developing technical insight for BGA interconnections at RF and microwave frequencies.

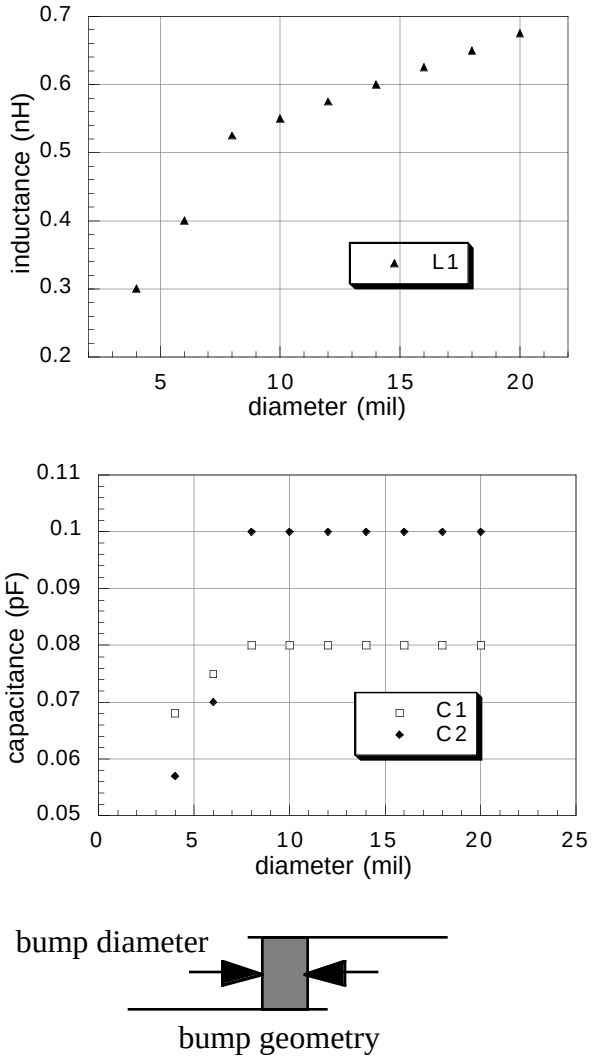


Fig. 7. Variation of lumped elements with the horizontal diameter of the bump.

Acknowledgment

This work has been supported in part by NSF Packaging Research Center at Georgia Tech under contract ECS-9402723.

References

[1] M.S. Cole, T. Caulfield, “A Review of Available Ball Grid Array (BGA) Packages”, *Proceedings of Surface Mount International Conference*, pp. 207-213, Aug. 1995.

[2] Hussein H.M. Ghouz and EL-Badawy EL-Sharawy, "An Accurate Equivalent Circuit Model of Flip Chip and Via Interconnects", *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 12, pp. 2543-2554, Dec. 1996.

[3] Carl Chun, Anh-Vu Pham, Joy Laskar and Brian Hutchison, " Development of Microwave Package Models Utilizing On-Wafer Characterization Techniques", *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 10, pp. 1948-1954, Oct. 1997.

[4] Robert W. Jackson and Ryosuke Ito, "Modeling Millimeter-Wave IC Behavior for Flipped-Chip Mounting Schemes", *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 10, pp. 1919-1925, Oct. 1997.

[5] M.P.R. Panicker, J.M. Hernandez, R.T. Griffin, D. Douriet, M. Sokol, "VIA/PAK™ BGA: A New Surface Mount Technology for Microwave Packaging, *Proceedings of 1995 International Electronics Packaging Conference*, pp. 11-20, Sept. 1995.